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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,647	10/19/2000	Martin McAfee	016295.0620 (DC-02500)	8276

7590 09/16/2003

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EXAMINER	
BADERMAN, SCOTT T	
ART UNIT	PAPER NUMBER
2184	3

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,647	MCAFEE, MARTIN	
	Examiner	Art Unit	
	Scott T Baderman	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The declaration states that the Applicant is the original, first and "joint" inventor of the subject matter which is claimed, however there is only "one (1)" inventor listed in the declaration.

Specification

2. After page 10 of the specification (i.e., the page where the claims begin), the pages are numbered from 1-6. Also, the Abstract page is numbered page 1. This is improper page numbering. The Examiner has renumbered the "Claim" pages numbers 11-16 and the "Abstract" page number 17. Any future amendments regarding these pages should refer to the renumbering of these pages.

Claim Objections

3. Claim 11 is objected to because of the following informalities: In lines 10 and 12, "corresponding" should be "first". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 5, 11 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As in claim 1, in lines 1-2, "possible microprocessors" is indefinite.

As in claim 5, it states that "if microprocessor is not present, then said switch provides as a switch output said debugging input to said corresponding microprocessor." How is debugging input provided to the corresponding microprocessor if the microprocessor is not present?

As in claim 11, in line 2, "possible processors" is indefinite.

As in claim 17, in line 1-2 and 5, "possible microprocessors" is indefinite.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter "AAPA") in view of Vivo (5,706,447) and Sanders et al. (6,249,832).

As in claim 1, AAPA discloses a debugging circuit capable of debugging a plurality of microprocessors that comprises a debug port and a plurality of microprocessor sockets, wherein each of the microprocessor sockets are adapted to receive a microprocessor, and wherein the plurality of microprocessor sockets are adapted to form a serial signal path (see pp.1-3 of the specification). Although AAPA discloses termination capabilities built into the CPU to ensure termination (see p. 2), AAPA does not disclose a plurality of switches, wherein each of the switches correspond to a respective one of the plurality of microprocessor sockets, and wherein each of the switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, and if a microprocessor is present, then the switch is automatically configured to include the microprocessor within the signal path, and if the microprocessor is not present, then the switch is automatically configured so that the signal path bypasses the corresponding microprocessor socket. Vivo discloses a system for automatically maintaining proper bus termination that includes a switch capable of automatically detecting whether a microprocessor (processor module) is present in the corresponding microprocessor socket, and if a microprocessor is present, then the switch is automatically configured (turned off) to include the microprocessor within the signal path, and if the microprocessor is not

present, then the switch is automatically configured (turned on) to include a termination device within the signal path (Figure 2, Abstract, column 4: line 27-53). Sanders discloses a bus termination system that connects a plurality of microprocessor sockets in an in-line topology, wherein the plurality of microprocessor sockets are connected serially so that the intermediate sockets that include terminator cards still allow signals (e.g., JTAG) to bypass the sockets until the signal reaches the bus end terminator (Figures 2 and 4, Abstract, column 2: lines 35-44, column 4: lines 7-40).

It would have been obvious to a person skilled in the art at the time the invention was made to include a plurality of switches, wherein each of the switches correspond to a respective one of the plurality of microprocessor sockets, and wherein each of the switches is capable of automatically detecting whether a microprocessor is present in the corresponding microprocessor socket, and if a microprocessor is present, then the switch is automatically configured to include the microprocessor within the signal path, and if the microprocessor is not present, then the switch is automatically configured to include a termination device within the signal path, into the system taught by AAPA above. This would have been obvious because Vivo clearly teaches that by including switches to automatically maintain bus termination prevents the need for additional manual intervention to reconfigure bus termination which increases the risk of a component being physically damaged (column 3: lines 34-44, column 4: lines 5-18).

It would have also been obvious to a person skilled in the art at the time the invention was made to modify the terminator cards taught above so that when a microprocessor is not present in the socket, a signal (e.g., JTAG signal) will still be able to pass through the terminator card (i.e., bypass the socket) onto the next socket, as was taught by Sanders above. This would

have been obvious because the circuit taught by AAPA is clearly designed to be able to debug the different microprocessors in the system, and Sanders clearly teaches of a similar circuitry, wherein microprocessor sockets are connected serially, and further clearly teaches of the transmission of a JTAG signal through the sockets, which is a well known debug/test signal. Further, Sanders clearly teaches that by connecting the microprocessor sockets serially with the terminator cards inserted in the empty sockets results in a more compact design and is easier to layout and route signal lines (column 4: lines 3-6).

As in claim 2, AAPA clearly teaches wherein a debugging input is provided to each microprocessor socket, and wherein a debugging output is provided from each microprocessor that is present in the corresponding microprocessor socket (see p. 2, lines 12-14 of the specification).

As in claim 3, Vivo discloses that each switch receives as an input a microprocessor detection signal indicating whether corresponding microprocessor is present (column 4: lines 49-53).

As in claim 4, Vivo discloses that when a microprocessor is present the switch will connect the microprocessor to the bus (Abstract), and AAPA discloses that when the microprocessor is present the microprocessor will provide a debugging output (see pp. 1-2 of the specification).

As in claim 5, Vivo discloses that when a microprocessor is not present the switch will connect the terminator card to the bus (Abstract), and Sanders discloses that the terminator card that is in place of a microprocessor will provide a JTAG signal to the next socket (Figure 2, column 4: lines 9-40).

As in claim 6, Sanders discloses that when a microprocessor socket does not contain the last microprocessor in the signal path, the JTAG signals continue to the next socket (Figure 2, column 4: lines 9-40), and AAPA discloses that when the microprocessor or terminator card is present, the microprocessor or terminator card will provide a signal to the subsequent microprocessor (see pp. 1-2 of the specification).

As in claim 7, Sanders discloses that the last microprocessor socket is connected to bus end terminators, and AAPA discloses that the signal passes through each successive microprocessor before returning to the debugging computer through the debug port (see p. 2 of the specification).

As in claim 8, AAPA discloses wherein the debug port is electrically coupled to a computer, receives input from, and provides output to the computer (see pp. 1-2 of the specification).

As in claims 9 and 10, AAPA, Vivo and Sanders disclose the system above. However, they do not clearly disclose that the switches comprise a pair of bipolar transistors or field effect transistors.

It would have been obvious to a person skilled in the art at the time the invention was made to include either a pair of bipolar transistors or field effect transistors as the switches taught above. This would have been obvious because Vivo clearly teaches that "any" switch device responsive to an enable type signal may be used (column 7: lines 40-45). A person skilled in the art would have understood that comprises a pair of bipolar transistors or field effect transistors are responsive to an enable type signal and could be used in the system taught by Vivo above.

As in claims 11 and 17, the Applicant is directed to claims 1, 3, 4 and 6 above.

As in claims 12, 13, 14 and 15, the Applicant is directed to claims 9 and 10 above.

As in claims 16 and 18, the Applicant is directed to claim 6 above.

As in claim 19, the Applicant is directed to claim 7 above.

As in claim 20, the Applicant is directed to claims 1 and 8 above.

As in claims 21 and 22, the Applicant is directed to claims 9 and 10 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Scott T Baderman
Primary Examiner
Art Unit 2184

STB